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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/940,709
Filing Date: August 28, 2001
Appellant(s): GSCHWIND ET AL.

Nathaniel T. Wallace
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 05, 2007 appealing from the Office action mailed June 04, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. Rejection of claims 22, 26, 29, and 33 under 35 USC 112, 1st paragraph is hereby withdrawn.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,678,790	Kumar	09-2004
6,321,318	Baltz	11-2001
6,868,472	Miyake	03-2005
2002/0087821	Saulsbury	7-2002
6,377,912	Sample	04-2002
6,611,796	Natarajan	08-2003
6,426,549	Isaak	07-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. Claim 29 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not support the claimed configurable memory with three modes of operation where any one of the modes is selectable at any time based on comparing an address to an address range contained in a configuration register. The closest support for this claim is the first full paragraph on page 23 (lines 3 – 17). This paragraph discloses that "the access mode of the configurable memory is selected based upon the address." The specification discloses only two modes of access for any given address - cache mode access and local memory mode access. In fact, it is unclear how a single address can operate in both cache and local memory modes at the same time as claimed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 8, 10 – 20, are rejected under 35 U.S.C. 102(e) as being anticipated by Kumar (US Patent No. 6,678,790).

4. With respect to claims 1 and 2, Kumar discloses a memory system on a chip (figure 1), comprising:

a configurable memory (16 + 12; see also figure 2, 13) having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (abstract), wherein the configurable memory comprises a memory array (12) in which both tag bits (figure 2, 50) and data bits (52) are stored in a single data line (col. 3, lines 32 – 33) in the memory array (figure 2, 12), in the second mode of operation, and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation (col. 2, lines 47 – 51).

5. With respect to claim 3, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a burn-in time (mode selection is under software control, making the mode selection possible anytime while the system is up and running, including "a burn-in time", i.e. a period of initial operation of a new device).

6. With respect to claim 4, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a power-up time (col. 2, lines 51 – 55).

7. With respect to claim 5, the first mode of operation or the second mode of operation is selected at the power-up time using an external signal (col. 2, lines 51 – 55).

8. With respect to claim 6, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution (col. 2, lines 47 – 48).

9. With respect to claim 7, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of a special configuration register (col. 2, lines 47 – 48).

10. With respect to claim 8, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal (col. 2, lines 48 – 51, control register is loaded by the CPU which is external to the memory).

11. With respect to claims 10 – 14, the configurable memory is **capable** of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses. (the claim only require a capability but not actual mode setting based on the addresses, this only requires that the structure can switch modes and can compare addresses, both of which are taught by Kumar; see comparator circuit 56 for example),

Dependent claims 11 – 14 relate to the capability discussed above.

12. With respect to claim 15, the configurable memory comprises:

a memory array (figure 2, 52); and

memory configuration logic for selecting the first mode of operation or the second mode of operation (figure 1, 16, figure 2, 58).

13. With respect to claim 16, the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation (read mode, i.e. mode of operation while reading, and write mode, i.e. mode of operation while writing, are inherent in this type of memory, either in cache mode or local memory mode).

14. With respect to claim 17, the selection may be overridden by the other selection dynamically (col. 2, lines 47 – 51).

15. With respect to claim 18, the configurable memory comprises a plurality of static random access memory cells (col. 3, lines 34 – 35).

16. With respect to claim 19, the configurable memory comprises a plurality of dynamic random access memory cells (col. 3, lines 34 – 35).

17. With respect to claim 20, the configurable memory is capable of being dynamically employed as a sole memory (abstract, main memory) serving the processor and as a portion of a larger, memory hierarchy (abstract, cache, see also col. 1, lines 18 – 24, cache is a portion of a larger memory hierarchy that includes a cache memory and a main memory).

18. Claims 1 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Saulsbury (US Patent Publication No. 2002/0087821).

Saulsbury discloses a memory system on a chip, comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory, wherein the configurable memory comprises a memory array in which both tag bits and data bits are stored in a single data line in the memory array, in the second mode of operation, wherein both modes of operations are employed concurrently (page 7, paragraph 67)

19. Claims 1, 10 – 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Baltz (US Patent No. 6,321,318).

20. With respect to claims 1 and 10 – 14, Baltz discloses a memory system on a chip (abstract), comprising:

a configurable memory (figures 1 and 9, 30 + 31) having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (abstract), wherein the configurable memory comprises a memory array (figure 9, 31 and 32) for storing tag bits and data bits in a single data line in the memory array, in the first mode of operation, wherein the configurable memory is **capable** of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses (claims only require a capability but not actual mode setting based on the addresses, this only requires that the structure can switch modes and can compare addresses, both of which are taught by Baltz; additionally, see col. 2, lines 38 – 46).

Dependent claims 11 – 14 relate to the capability discussed above.

21. With respect to claim 21, Baltz discloses that the first mode of operation and the second mode of operation are employed concurrently (col. 9, lines 9 – 10).

22. Claims 1 – 3, 6 – 10, 13 – 17, 20 – 23, 25, 26, 29, 30, 32, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyake et al. (US Patent No. 6,868,472, hereinafter "Miyake).

23. With respect to claims 1, 2, 6 – 10, 13 – 17, 20 – 23, 25, 26, Miyake discloses a memory system on a chip for accessing data, comprising:

a configurable memory having a first mode of operation wherein the configurable memory (figures 35 and 37, 320) is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (col. 34, lines 40 – 50), wherein the configurable memory comprises a memory array for storing tag bits (307) and data (326) bits in a single data line in the memory array, in the first mode of operation,

wherein the first mode of operation or the second mode of operation is selected during the program execution based upon comparing (figure 38, 347) a supplied address (figure 38, addr supplied to 347) to at least one address range contained in at least one configuration register (345; see also col. 37, lines 7 – 26, 40 – 61) and generating a control signal (control signal generated by 347 and 353) based on said comparison to select the first or second mode of operation (col. 37, lines 7 – 26, 40 – 61; when an address that corresponds to the configured RAM region is supplied, the cache memory configured as RAM emulates RAM by responding to specific location access request).

24. With respect to claim 29, as shown above, Miyake's configurable memory supports, cache, RAM, and cache/RAM hybrid modes and uses address comparator to compare a supplied address to an address range stored in a register to select a mode of operation.

25. With respect to claims 30, 32, and 33, Miyaki discloses a method for accessing data, comprising the steps of:

providing a configurable memory in a package (col. 34, lines 45 – 46);

providing control logic in the package for selecting between a first mode of operation and a second mode of operation of the configurable memory and for overriding a previous selection of the first mode of operation or the second mode of operation (col. 34, lines 55 – 65);

configuring the configurable memory as a local, non-cache memory in the first mode of operation;

configuring the configurable memory as a cache in the second mode of operation, wherein the configurable memory comprises (figure 35, 320) a memory portion for storing tag (figure 37, 307) bits and data bits (326) in a single data line in the memory portion, in the second mode of operation; and

accessing the data from the configurable memory, based upon a mode of the configurable memory,

wherein either the first mode of operation or the second mode of operation is selectable during a program execution based on comparing a supplied address to at least one address range contained in at least one configurable register and generating a control signal based on said comparison to select the first or second mode of operation (col. 37, lines 5 – 18, Miyake discloses using only a portion of the cache in RAM mode and assigning an address range corresponding to the cache memory acting as the RAM; lines 40 – 47, Miyake also discloses generating a control signal based on the comparison to generate a control signal to operate the cache/RAM just as applicant discloses).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mikaye in view of Sample *et al.* (US Patent No. 6,377,912, hereinafter "Sample"), or in the alternative, in view of Natarajan (US Patent No. 6,611,796).

Miyake discloses all of the limitations of the parent claim as discussed above. However, Miyake does not specifically disclose macro cells to implement memory system. On the other hand, Sample (col. 29, lines 11 – 17, col. 31, lines 27 – 33) and Natarajan (col. 4, lines 16 – 23) disclose the use of macro cells in IC memory chip designs.

It would have been obvious to one of ordinary skill in the art, having the teachings of Miyake and Sample or Natarajan before him at the time the invention was made, to use the design techniques using macros teachings of Sample or Natarajan in the design of Miyake's system, in order to be able to verify electronic circuit designs before fabrication (Sample 16 – 18, Natarajan 23 – 26).

28. Claims 27, 28, 31, 34 - 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Isaak (US Patent No. 6,426,549).

Miyake discloses all of the limitation of the parent claim as discussed above. However, Miyake does not specifically disclose methods of integrating the claimed memory package using a chip stack and a flip chip techniques. On the other hand, Issak discloses both of these techniques (abstract).

It would have been obvious to one of ordinary skill in the art, having the teachings of Miyake and Isaak before him at the time the invention was made, to use the IC packaging teachings of Isaak to make the configurable memory IC of Miyake, in order to be able to actually produce the memory devices. Isaak's method uses available materials and known process techniques and is suitable for automated production methods (col. 3, lines 49 – 53).

(10) Response to Argument

Rejection of Claim 29 under 35 USC 112, 1st paragraph

Appellant contends that the statement in the specification "[t]hese control logic components enable, for example, four modes of operation: local memory read mode; local memory write mode; cache read mode; and cache write mode" supports the limitation "a configurable memory having three modes of operation, a first mode of operation for emulating local, non-cache memory, a second mode of operation for emulating a cache, and a third mode of

operation for emulating both the local memory and the cache." (Appeal Brief, pp. 9-10). However, Appellant does not explain which of the four modes of operation (read local, write local, read cache, write cache) disclosed in the specification correspond to each of the three modes of operation that are claimed (local memory, cache memory, both local and cache memory). Appellant is unable to explain this because the three recited "modes" relate to the configuration of the memory (all cache, all local memory, or part cache and part local memory), while the four modes of operation disclosed in the specification relate to the memory "access modes". Appellant conflates memory configuration and memory access by referring to both using the same term "modes of operation" resulting in a claim that is not operable.

Appellant contends that the following passage in the specification (p. 23, ll. 3-17) supports claim 29 (see Appeal Brief, pp. 10-11):

> Yet another exemplary configuration option is as follows. When the CPU 110 performs a memory access, the access mode of the configurable memory array 130 is selected based upon the address of the memory access (step 550). For example, when the CPU 110 performs a memory access, the supplied address of the access determines whether the memory array is to be treated as local memory or cache. This can be used to effectively partition the configurable memory array 130 into (1) a small high-speed local working memory for data processing and (2) a cache for access to a large system memory. The control information may be obtained by comparing the address to one or more address ranges contained in configuration register(s) (step 550a), or by performing any of a variety of logical operations on the address bits (step 550b).

The **access mode** disclosed above is based upon the address of the memory access. A given location in the array is treated as local memory or cache depending on the address based on comparing the address to address ranges contained in the configuration register. In contrast, the three modes recited in the claim relate to how the memory is configured (all local memory, all cache, or part cache and part local memory). While the array may be configured to operate as

part cache and part local memory, any give location must operate either as local or cache memory. One skilled in the art understands that a single memory location cannot support both access modes at the same time because local memory and cache memory operate in fundamentally different ways. Local memory locations must be addressed specifically and individually for access whereas individual cache memory locations are not specifically addressable (because cache contains data for other specifically addressed system memories and provide fast storage on behalf of other specifically addressable system memory locations responding to the system memory addresses rather than having its own addresses). A local memory location stores data specifically intended to be stored at that location while a cache memory location contains data intended for other memory locations. Contents of local memory cannot change by read operations while cache memory contents change when there are read cache misses.

Anticipation of Claim 1 by Kumar

The only issue raised by Appellant is whether Kumar teaches the limitation "a memory array in which both tag bits and data bits are stored in a single data line in the memory array." Appellant does not dispute that Kumar teaches storing a single logical data line, where the logical line comprises tag bits and data bits (in a cache that uses tags to retrieve cached data, there is a one-to-one correspondence between a tag and its corresponding data, forming a single logical line that comprises both tag and data, as specifically disclosed by Kumar at col. 3, lines 32 – 33). Instead, Appellant argues that Kumar's teaching of storing "a single logical data line" that comprises both tag and data in a memory array 12 is not on point and seemingly irrelevant

when the disputed limitation is based on Appellant's disclosure of storing a tag and data in a **single logical line** in a memory array. The Examiner notes that the basis for the disputed limitation can be found at page 5, lines 11 – 14, of the specification where Appellant discloses that "[t]he configurable RAM **array** has a memory portion for storing tag bits and data bits in a **single logical line** in the second mode of operation." Removing the word "logical" to make the claim broader does not make the term "a single logical line" irrelevant or not on point, when that term is the basis for the claimed limitation.

Appellant's only real argument seems to be that because Kumar discloses a configurable memory array 12 that comprises a separate tag array 50 and data array 52 (Kumar figure 2), Kumar does not anticipate the claim. The Examiner notes that the limitation "memory array" can be reasonably interpreted in light of the specification in two different ways. A broader interpretation of the limitation "a memory array" is that of a functional unit that comprises physical memory cell arrays and control circuits, such as Kumar's memory array 12 or Appellant's memory array 130. A narrower interpretation of "a memory array" is a single physical memory array, such as Saulsbury's DRAM memory bank 14 (discussed below) or Appellant's memory array 410.

The broad interpretation that includes Kumar's memory array 12 is supported by Appellant's specification. Figure 1 of the Appellant's disclosure shows a configurable **memory array** 130. As discussed above this memory array 130 stores tag bits and data bits in a single logical line. In the paragraph starting at page 17, line 21, Appellant describes the cache mode

operation of the configurable **memory array** 130 with the last sentence disclosing two different embodiments of this memory array 130, one of which includes separate arrays for storing data and tags (page 18, lines 10 – 14, "In the preferred embodiment, cache tags are included in data lines stored in the memory array 410, but alternate implementations can include separate memory arrays for storing data and tags"). Thus, in at least one embodiment, Appellant's **memory array** 130, that stores tag bits and data bits in a single logical line, comprises separate tag and data arrays just like Kumar's **memory array** 12, which comprises a tag array 50 and a data array 52. Appellant's own disclosure conclusively shows that Appellant's use of the term "**memory array**" is not limited to a single physical array, as Appellant seems to be arguing, but can comprise one or more other arrays (or subarrays).

Appellant points to the same portion of the specification (page 18, lines 10 – 14) to argue that that there is a difference between cache tag being stored in data lines stored in a memory array and having separate memory arrays for storing data and tags. The Examiner agrees that there is a difference. However, the Examiner does not agree that the second embodiment with separate tag and data arrays is not covered by the claim language because Appellant used the term "memory array" in a way that encompasses a memory array that include other memory arrays. The Examiner also notes that the sentence at page 18, lines 10 – 14 ("... cache tags are included in data lines stored in the memory array 410 ..."), does not provide textual support for the claimed limitation "both tag bits and data bits are stored in a **single data line**." The support for the "single data line" limitation can only be found in the portion of the specification that discussed the configurable memory array 130 as a whole.

Anticipation of Claim 1 by Baltz, and Mikaye

Appellant's arguments regarding Baltz and Miyake references are essentially the same as arguments against Kumar. Both Baltz and Miyake disclose storing both tag and data in a single logical data line of a memory array that comprises tag and data arrays. Appellant's arguments fail for the reasons discussed above.

Anticipation of Claim 1 by Saulsbury

The Examiner initially notes that Saulsbury anticipates the claim under the narrower interpretation of "a memory array." Appellant argues that Saulsbury's general statement that a DRAM memory can be configured as "a cache memory with associated tags" does not teach or suggest the claimed limitations of "a memory array in which both tag bits and data bits are stored in a single data line in the memory array" (Appeal Brief, page 17) while Appellant is relying on the general statement in the specification that "cache tags are included in the data lines stored in the memory array" to support Appellant's arguments (Brief, page 15) and the claim language. As discussed above, tag bits and corresponding data bits form a data line. Saulsbury specifically discloses that memory 14 comprises RAM memory and can be configured as cache memory with associated tags or as directly accessible physical memory (page 7, paragraph 67).

Appellant's discussion of caches with separate data and tag arrays shown in figure 3 is irrelevant and misleading, as figure 3 is a figure of the processor core 12 shown in figure 1 (see figures and page 2, paragraph 16), not the configurable memory 14. Moreover, as discussed above, Appellant's definition of a memory array includes an array that contains other arrays.

Anticipation of Claims 10, 13, and 14 by Mikaye

Appellant's only argument regarding these claims is that they depend from claim 1, which was shown to be anticipated as discussed above. Therefore, Appellant has not overcome the rejections based on the teachings of Miyake.

Anticipation of claims 10 – 14 by Kumar and Baltz

Claim 10 recites the limitation "wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses." Appellant does not dispute that Kumar and Baltz separately disclose a configurable memory capable of operating in cache mode or local memory mode. Appellant argued "[t]his provides clear support for claim language that a mode selection can be performed by a particular method, **but not required to be performed by such method**" (Brief, page 16). By Appellant's own admission, Appellant does not intend the mode selection based on address comparison "feature" to be a required feature of the claim. Kumar clearly discloses selecting a mode of operation based on a control signal (figure 2, 36), and the claim does not require that the control signal be generated by address comparison. Kumar's configurable memory is capable of responding to a control signal generated by address comparison so long as the generated signal is the same type of signal as the control signal 36.

Anticipation of claims 2 – 8 and 15 – 20 by Kumar

Appellant has not made a separate argument regarding these claims. Therefore, Appellant has failed to overcome the rejection of these claims because Appellant has failed to overcome the rejection of their parent claim as shown above.

Anticipation of claims 22, 26, 29, 30 and 33 by Mikaye

Appellant's only allegation is that Miyake does not specifically disclose "comparing a supplied address to at least one address range contained in at least one configuration register and generating a control signal based on said comparison to select one of the modes of operation." Appellant offers no real argument or explanation to support the allegation. Miyake discloses a two way cache where 1) both ways can act as regular cache memory (col. 36, lines 47 – 49), 2) both ways can act as RAM (col. 36, lines 49 – 50, col. 37, lines 5 – 7), or 3) one way configured as cache and one way as RAM (col. 37, lines 7 – 9). When Miyake's configurable cache way is configured as RAM, address range for the RAM must be specified and stored in the RAM address register 345 (Figure 38). This hybrid cache/RAM configuration necessarily requires address comparison because as explained above, while a cache memory location is not directly accessible to the memory requesters and does not have its own unique address, each RAM location must be addressable with a unique address. In order to operate a portion of cache memory as RAM, the configurable memory controller must determine whether memory location being accessed is in the region of the memory configured as RAM. This determination can only be made by comparing address being accessed with the address range configured for the configurable RAM. This necessary address comparison feature of configurable cache/RAM memory is expressly disclosed by Mikaye in Figure 38 and col. 37, lines 49 – 60, where Miyake

describes the details of how the configurable cache (figure 37) emulates RAM when the address comparator 347 decides that there is a match between a requested address (claimed as "supplied address") and the configured RAM address (col. 37, lines 49 – 52).

Rejections of claims 24, 27, 28, 31, 34 – 37 under 35 USC 103

Appellant's only argument is that these claims depend from the respective independent claims. As discussed above, Mikaye anticipates the parent claims. Therefore, Appellant has failed to overcome the rejections.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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